High Efficiency 28V Class AB InGaP/GaAs HBT MMIC Amplifier with Integrated Bias Circuit

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Abstract — **InGaP/GaAs HBT has demonstrated excellent lifetime and linearity performance for 3 to 10V operation. This is very attractive to infrastructure application. However the low voltage is a drawback in this application where 28V is a common voltage used. In this effort, high voltage InGaP/GaAs HBT is developed for 28V operation. Safe operation area is carefully designed allowing the device to function in class A mode. Thermal resistance of 30°C/W for a 1W HBT design is measured using the V_{be} method. 4W CW power with 71% efficiency is measured from this 1W design, with a junction temperature rise of 49 °C. The integrated temperature compensated bias circuit provides <9% quiescent current change over base plate temperature from -40 to +85°C . Two Tone and CDMA2000 linearity is characterized. Initial WLR (wafer level reliability) result indicates that it has similar lifetime as the standard InGaP/GaAs HBT.**

I. Introduction

InGaP/GaAs HBT has achieved great reliability [1] in lifetime test as well as good linearity. Both features are critical to the infrastructure application.

However infrastructure usually requires higher voltage operation than the conventional GaAs HBT could handle. 28V is a commonly used voltage in infrastructure to provide the necessary power level and reduces the electrical current at the same RF power level. Several works were reported on the high voltage GaAs HBT [2,3]; 28V operation was demonstrated with multi-watts output power. But these works require more exotic approach to reduce the thermal resistance; the safe operation area was not studied either.

In [2] a 10°C/W thermal resistance of this flip chip approach was measured by IR method. At 15W output power level a temperature rise of 100 °C is estimated accordingly. In [3] although front side thermal shunt technique is used, the thermal resistance was not mentioned.

The present work focused on achieving low thermal resistance with a good SOA (safe operation area) in the conventional MMIC approach. 30°C/W thermal resistance was measured for a 1W class A design. This MMIC chip includes the input matching circuit and a temperature compensated bias circuit. The bias circuit allows the user to set the amplifier in different class of operation, from class A to near class B.

4W CW power in class AB operation was achieved from a 1W class A design. The temperature rise is only 49°C. Linearity in two tone and CDMA2000 is characterized as well. A 3:1 VSWR output mismatch was achieved in this matching condition.

This work demonstrated that 28V InGaP/GaAs HBT could be put into production in the same manner as the conventional MMIC.

II. Semiconductor Technology

A. HBT device

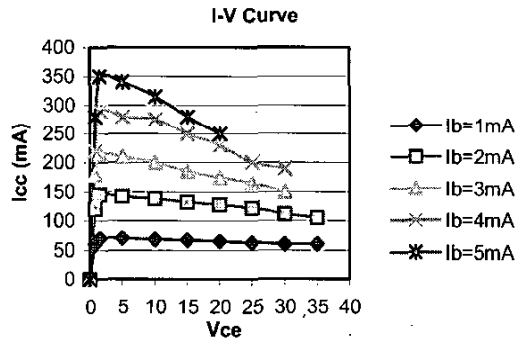

Fig. 1. Measured I-V curve of a multi-finger HBT. The emitter area is 1500μm². Good SOA is established.

Conventional InGaP/GaAs HBT has a collector thickness usually in the 0.5 to 1.0μm range, providing a BV_{cbo} less than 30V. To achieve higher breakdown voltage, a 3μm thick collector is used. The base and emitter layers are essentially identical to the standard HBT. The collector is designed to be fully depleted to improve the linearity [4]

The device is processed in the same way as the conventional low voltage counterpart except the collector

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etching. 70V BV_{cbo} is achieved with this structure; the BV_{ceo} is >30V allowing the DC bias as high as 30V. Figure 1 is the I-V curve measured on an assembled IC die. The emitter junction area is about 1500μm^2.

B. Thermal resistance and ballasting design

Thermal resistance design is always the first task for any power device. In this work, no special thermal resistance reduction method is adopted. Sufficient spreading of the active HBT fingers across the IC die is required in the conventional MMIC approach. The substrate is kept at 100μm thick. Although class AB operation is common in many high voltage device (Silicon bipolar and Silicon LDMOS), class A operation condition is considered essential in the present work. Class A operation provides improved linearity at the power back off state, which is important for driver stages or error correction stages.

The ballasting is critical in any bipolar transistor design. A proprietary program is used in the design. As shown in Figure 1, the power HBT can be biased to 30V with current up to 190mA (12.3kA/cm^2 current density). The total DC power dissipation is 5.7W. The design is intended for a 1W class A operation, i.e. for a 2W power dissipation assuming 50% efficiency. It validates the design algorithm and provides the margin for the operation.

C. Initial reliability study

Since the high voltage HBT will run at lower current density than the conventional HBT, the current gain degradation is expected to be less a problem. Wafer level reliability study was done first. The device was stressed at 6V V_{ce} and 200kA/cm^2 current density on a 2x6μm^2 finger. 33 hours lifetime was achieved, which is very similar to the low voltage InGaP/GaAs HBT result [5].

III. Design, Assembly, and RF Evaluation

A. RF Circuit Design

Figure 2 shows the basic circuit design. The input matching circuit is implemented in a low pass configuration made of on-chip inductor and MIM capacitor. The output matching circuit is not included on the chip; it would be realized in the hybrid approach for easy adjustment.

A temperature compensated bias circuit, based on the current mirror approach, is included. Figure 3 shows the measured DC quiescent current over the –40 to +85°C base plate temperature range. Less than 9% quiescent current change is achieved over this broad temperature range. This greatly helps to maintain the RF performance over temperature. The on-chip bias circuit also reduces the trouble in design and matching the temperature behavior between bias and RF transistors.

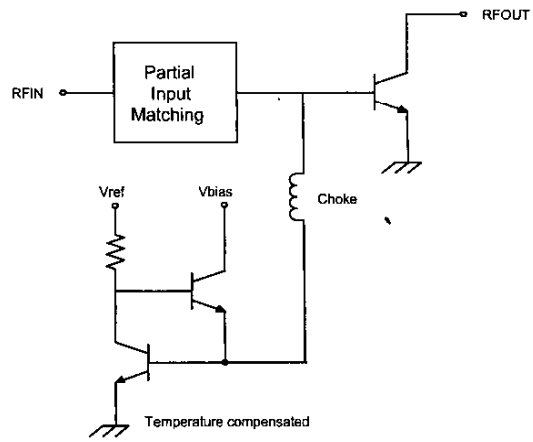

Fig. 2. Basic circuit design of the MMIC amplifier is displayed. The bias circuit is based on current mirror design.

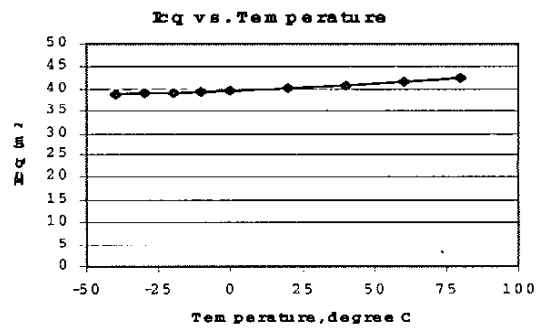

Fig. 3. Measured quiescent current over base plate temperature from –40 to +85°C: Less than 9% change is achieved.

B. Assembly and RF Evaluation

The IC die is eutectic mounted onto a gold plated Molybdenum carrier, which is in turn soldered onto the heatsink through the cutout of the RF test board. Gold bonding wire connects the HBT MMIC to the test board. The output matching was achieved by matching circuit on the PCB. Surface mount matching components were used to realize the output matching circuit.

The RF performance evaluation was made by the adjustment of the values of the matching components.

The RF signal is measured at the SMA connectors and no correction is made to account for the matching circuit loss.

IV. Performance

A. Thermal Resistance

The thermal resistance is measured using the V_{be} method [6]. For the 1W design assembled according to III.B method, a 30°C/W thermal resistance was measured. This is in line with the design. For a 2W power dissipation, the device junction temperature rise will be maintained at 60°C.

B. CW RF Gain and Power

The amplifier is evaluated at 900MHz. Figure 4 shows the gain and power performance. 36dBm is achieved with 14dB associated gain from a 1W design. Efficiency, defined as output power over the total DC input power (including the power into the bias circuit), reaches 71%; while the PAE is at 68.2%. The amplifier is biased at $28V_{cc}$ in class AB mode with a 40mA quiescent current. The maximum gain is 18dB at 34dBm output power.

At 36dBm output power, the temperature rise is 49°C. This low temperature rise is a result of the high efficiency and the conservative thermal design.

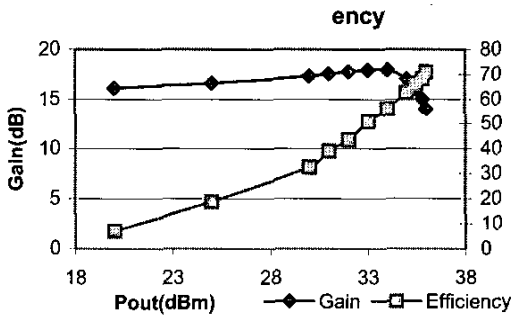

Fig. 4. Gain and efficiency versus output power for the $28V_{cc}$ operation of HBT MMIC.

The load impedance for 4W output power is measured. The real part is 78Ω (in the parallel configuration of resistor and inductor). From the simple equation of

$$Power=V_{rf}^2/(2*R_{load})$$

the V_{rf} is estimated to be 25V. Since the loss of the output matching circuit is not included, it shows that there is no "dead zone" in the knee voltage region of the I-V curve.

Output mismatch experiment was done. The amplifier was driven to 4W output power, and then the output mismatch up to 3:1 VSWR for all phases was applied. The amplifier passed the test without any damage.

C. Linearity

The linearity performance of the HBT MMIC is evaluated over two-tone test and CDMA2000. The output matching was readjusted for the best linearity performance. The maximum power with a single tone signal is about 33.5dBm.

Figure 5 is the two tone result. Tests on both class A (I_{cq}=120mA) and class AB (I_{cq}=40mA) bias conditions are shown. Class AB bias shows a sweet spot in IM3 near the maximum power level. Class A does not show this sweet spot. At further backoff of power class A shows superior IM3 and IM5 result over class AB.

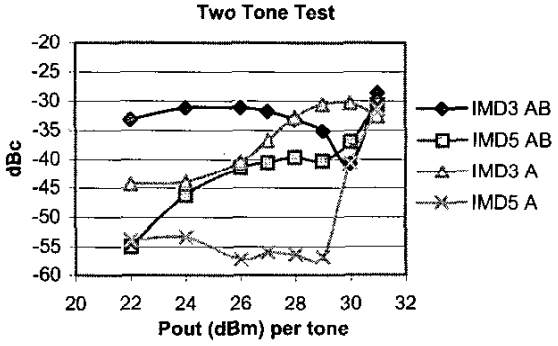

Fig. 5. Two tone result for both class A and class AB operations.

Figure 6 is the result of CDMA2000. 9 forward channel signal is used. The peak-to-average ratio is about 8.5dB. ACLR is shown to deteriorate rapidly at the high power level due to the waveform clipping (peak power exceeds the maximum power of the amplifier). Class A again shows better ACLR than class AB at the backoff power level. Class AB shows a slight "sweet spot" around 27dBm. Figure 7 is the plot of the efficiency associated with the test conditions in figure 6. Class AB shows improved efficiency throughout the whole power range. 35% efficiency is achieved in class AB operation when ACLR reaches –45dBc.

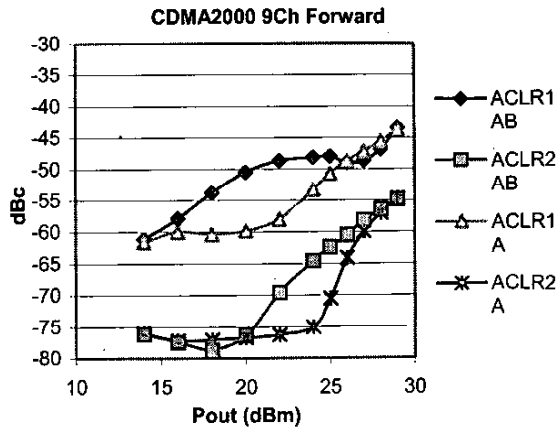

Fig. 6. ACLR of CDMA2000 9 channel Forward Link for class A and class AB operations

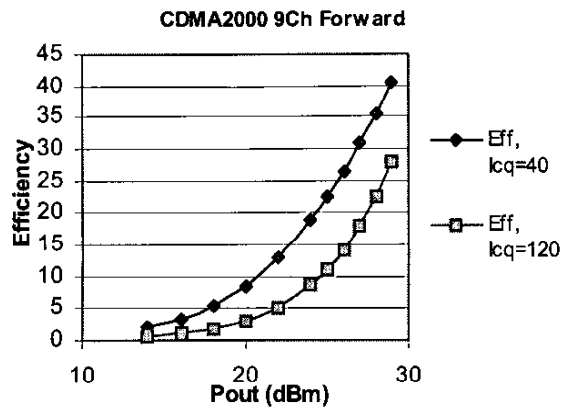

Fig. 7. Efficiency of CDMA2000 9 channels Forward Link for class A and class AB operations

V. Conclusion

Initial result of 28V InGaP/GaAs amplifier is presented. The design uses conventional MMIC approach with input matching and bias circuit built on chip. SOA is established validating the proprietary design technique. The MMIC amplifier assembled into an evaluation circuit was tested. 4W output power was achieved with 71% efficiency. Linearity was evaluated by two tone and CDMA2000. ACLR at –45dBc was achieved with 35% efficiency.

Acknowledgement

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References

[1] B. Lin,"InGaP HBTs offer Enhanced Reliability," Applied Microwave & Wireless, pp. 115-116, Dec. 2000

[2] D. Hill, T.S.Kim, "28V Low Thermal-Impedance HBT with 20W CW Output Power," *IEEE Trans. Microwave Theory and Tech.*, vol. MTT-45, no. 12, pp.2224-2228, Dec 1997.

[3] P.Kurpas et al, "High-voltage GaAs Power-HBTs for Base-Station Amplifiers," 2001 *IEEE MTT-S Int. Microwave Symp. Dig.*, pp. 633-636, June 2001.

[4] N.L. Wang, W.J.Ho, J.A. Higgins, "AlGaAs/GaAs HBT Linearity Characteristics," *IEEE Trans. Microwave Theory and Tech.*, vol. MTT-42, no. 10, pp.1845-1850, Oct. 1994

[5] H.F.Chau et al, "Wafer level reliability tests of InGaP HBTs using High Current Stress," 2002 *IEEE GaAs Mantech Dig.*

[6] D.E. Dalson et al, "CW measurement of HBT Thermal Resistance," *IEEE Trans. Elec. Dev. 39-10*, pp. 2235-2239, 1992.